

CLAIMS

What is claimed is:

Subm 7
1 1. A system comprising:
2 a direct memory access (DMA) controller; and
3 an input/output (I/O) device coupled to the DMA controller, wherein the
4 DMA controller is adaptable to terminate a DMA transfer before a terminal
5 count is reached.

003242.P014
1 2. The system of claim 1 wherein the DMA controller is adaptable to re-
2 execute a DMA transfer with the I/O device.

1 3. The system of claim 1 wherein the DMA controller is adaptable to operate
2 in a normal mode and a descriptor mode

1 4. The system of claim 3 wherein the DMA controller executes a series of
2 single transfers to the I/O device while operating in the descriptor mode.

1 5. The system of claim 4 wherein the DMA controller is adaptable to
2 automatically determine the sequence of the single transfers to be performed
3 while operating in the descriptor mode.

Subm 7
1 6. The system of claim 1 further comprising:
2 a system interconnect coupled to the I/O device and the DMA controller;
3 a central processing unit (CPU) coupled to the system interconnect; and

4 a memory device coupled to the system interconnect.

1 7. The system of claim 1 wherein the DMA controller comprises:
2 one or more DMA channels; and
3 a configuration register matrix coupled to one or more DMA channels.

1 8. The system of claim 7 wherein each of the DMA channels comprises:
2 control logic; and
3 descriptor logic.

1 9. A system comprising:
2 a direct memory access (DMA) controller; and
3 an input/output (I/O) device coupled to the DMA controller, wherein the
4 DMA controller is adaptable to operate in a normal mode and a descriptor mode.

1 10. The system of claim 9 wherein the DMA controller is adaptable to re-
2 execute a DMA transfer with the I/O device.

1 11. The system of claim 9 wherein the DMA controller is adaptable to
2 terminate a DMA transfer to or from the I/O device.

1 12. A system comprising:
2 a direct memory access (DMA) controller; and
3 an input/output (I/O) device coupled to the DMA controller, wherein the
4 DMA controller is adaptable to re-execute a DMA transfer with the I/O device.

1 13. A method comprising:
2 transferring data between a first device and a second device under control
3 of a direct memory access (DMA) controller;
4 receiving a request signal at the DMA controller from the first device,
5 wherein the request signal indicates a request by the first device to re-transmit
6 the data between the first device and the second device;
7 transmitting an acknowledge signal from the DMA controller to the first
8 device; and
9 re-transferring the data between the first device and the second device.

1 14. The method of claim 13 further comprising reloading configuration
2 registers within the DMA controller prior to transmitting the acknowledge signal
3 to the first device.

1 15. A method comprising:
2 transferring data between a first device and a second device under control
3 of a direct memory access (DMA) controller;
4 receiving a request signal at the DMA controller from the first device,
5 wherein the request signal indicates a request by the first device to terminate the
6 transfer of data between the first device and the second device;
7 transmitting an acknowledge signal from the DMA controller to the first
8 device; and

7A1
9 terminating the transfer of data between the first device and the second
10 device.

1 16. The method of claim 13 further comprising clearing a counter within the
2 DMA controller prior to transmitting the acknowledge signal to the first device.

1 17. A method of executing a direct memory access (DMA) transfer
2 comprising:
3 retrieving a first set of commands from a descriptor table at a DMA
4 controller;
5 receiving a first request signal at the DMA controller from the first device,
6 wherein the request signal indicates a request by the first device to transfer data
7 between the first device and a second device under the control of the DMA
8 controller;
9 transmitting a first acknowledge signal from the DMA controller to the
10 first device; and
11 transferring data between the first device and the second device according
12 to the first set of commands.

1 18. The method of claim 17 further comprising constructing the descriptor
2 table within a memory device.

1 19. The method of claim 17 further comprising programming the first set of
2 commands in to configuration registers within the DMA controller after
3 retrieving the first set of commands.

1 20. The method of claim 17 further comprising:
2 determining whether more commands are stored in the descriptor table; if
3 so,
4 retrieving a second set of commands from the descriptor table;
5 receiving a second request signal at the DMA controller from the first
6 device;
7 transmitting a second acknowledge signal from the DMA controller to the
8 first device; and
9 transferring data between the first device and the second device according
10 to the second set of commands.

1 21. The method of claim 17 further comprising:
2 receiving a second request signal at the DMA controller from the first
3 device, wherein the second request signal indicates a request by the first device
4 to re-transmit the data between the first device and the second device;
5 transmitting a second acknowledge signal from the DMA controller to the
6 first device; and
7 re-transferring the data between the first device and the second device
8 according to the first set of commands.

1 22. The method of claim 17 further comprising:
2 receiving a second request signal at the DMA controller from the first
3 device, wherein the second request signal indicates a request by the first device
4 to terminate the data between the first device and the second device;
5 transmitting a second acknowledge signal from the DMA controller to the
6 first device; and
7 terminating the transfer of data between the first device and the second
8 device.

1 23. The method of claim 22 further comprising:
2 reducing a transfer count within the descriptor table after terminating the
3 transfer; and
4 retrieving a second set of commands from the descriptor table;